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ADC Crosstalk Measurements with SNAP for OVRO-LWA

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ADC Cross-Talk: Initial Measurements with Test Board

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I. Introduction

A PCB has been constructed for testing analog-to-digital converter ICs and their input circuits. It includes two Analog Devices HMDAC1511 (called devices B and D) and two Texas Instruments ADS5296A devices (A and C), each of which can digitize 4 signals at 200 MSa/s. They provide 8b per sample and 10b per sample, respectively. For each IC type, one is connected to its analog inputs using differential signaling via an ARJ45 connector, and the other is connected using single-ended (coax) signaling via four MMCX connectors and on-board baluns. The baluns use 1:2 impedance-ratio transformers and all signals are terminated in 100 ohms (differential) at the ADC device. The board layout allows for selecting any of several balun circuit topologies by replacing resistors.

The board design is based on that of the CASPER ADC16x250. It has the same form factor and its digital outputs and power use a ZDOK connector, compatible with the ROACH2 FPGA board. Differences include providing bit clock and frame clock from one HMDAC1511 and one ADS5296A (vs. bit clock only), and supporting the ADS5296A's register readback feature.

This report gives some initial test results. Crosstalk among the 8 signals into the two HMDAC1511 devices was measured. Tests involving the ADS5296A devices await necessary modifications to the available FPGA code.

II. Methods

FPGA code provided by Jonathon Kocz allows capturing 65,536 consecutive samples from each of the four signals digitized by one device. Those captured samples were used for these tests. All ADCs were clocked at f_c = 200.0 MHz using a Valon 5009 synthesizer.

A single tone at f_1 = 34.179716 MHz was delivered to one of the inputs at nearly full-scale (+7 dBm) and detected at all 8 outputs. The other 7 inputs were driven with a weaker signal (–6.8 dBm) at f_2 = 97.437423 MHz for "dithering"; this allows accurate measurement of the power in a signal weaker than 1 LSB, as was usually the case for the cross-talk signals. Otherwise, such a weak signal would either not be seen at all (output is constantly zero) or would appear to have an amplitude of 1/2 LSB, even though it is much weaker, depending on the d.c. offset of the ADC. The test signal at f_1 was provided by a Hittite HMC-T2220 synthesizer, and the dither signal at f_2 was provided by the second synthesizer in the Valon 5009. All three signals were locked to the same 10 MHz reference, provided by the HMC-T2220. Both frequencies were chosen to have an integer number of cycles in 65,536 samples.

The power at f_1 was determined from the captured samples using a software I-Q mixer:

$$I = \mathrm{sum}[s_i \cos(2\pi f_1 i/f_c)]$$
$$Q = \mathrm{sum}[s_i \sin(2\pi f_1 i/f_c)]$$
$$P = I^2 + Q^2$$

where s_i is the ith sample (8b integer) and the sum is over all samples. This effectively discriminates against the dither signal. Measurements in which the test signal was turned off but the dither signal remained on gave residual power 90 to 100 dB below the test signal, which is in agreement with the expected quantization noise.. With the test signal on, if the I-Q mixer replaces f_1 with $f_1 + f_c/32768$, the apparent power is again 90 to 100 dB lower.

The differential input signals into the ARJ45 connector were delivered via a SMA-to-ARJ45

breakout board and a 1 m CAT7 cable with ARJ45 plugs. The breakout board contains 1:2 impedance transformers as baluns. These are the same transformers as are used on the ADC board for the coax channels.

A photograph of part of the test setup is shown in Figure 1. A later version of this report will provide a detailed block diagram.

III. Results

Figure 2 shows a typical set of histograms of the samples from all 8 channels when the test signal was applied to channel 8. Channels 1-4 are the coax inputs to ADC chip B (also called B1-B4), and 4-8 are the differential inputs to chip D (also called D1-D4).

The cross-talk results are shown in Table 1.

IV. Discussion

The apparent cross-talk ranged from –52.7 to –68.7 dB. This is disappointing, since the IC data sheet claims typical cross-talk of –70 dB, and measurements on a SNAP board using a similar method [1] gave cross-talk with average was near –86 dB and worst-case of –71 dB.

There was no clear difference between the within-chip cross-talk and the chip-to-chip cross-talk, but the results were 3 to 10 dB better when the test signal was applied to a coax input than when it was applied to a differential input.

If cross-talk is entirely due to passive coupling, then it should be reciprocal, but the results show poor reciprocity. The difference is less than 2 dB among differentially-connected signals (D1-D4), but as much as 6 dB among coax-connected signals, and up to 8 dB between signals to different chips

Results in these tests were not very repeatable. In one set of measurements with the test signal into D3, the results were 20 to 30 dB better than in Table 1 for unknown reasons. Most other paths repeated within 3 dB and many repeated within 1 dB. This needs further investigation.

Reference

[1] J. Atwater, L. D'Addario, and J. Kocz, "ADC Crosstalk Measurements with SNAP for OVRO-LWA." OVRO-LWA internal report, 2018 Sep 13.

Table 1: ADC Test Board: Measured Cross-Talk at 34.2 MHz, dB

in \ out	B1	B2	B3	B4	D1	D2	D3	D4	max	min
B1		-65.94	-61.11	-62.73	-57.80	-56.66	-60.87	-62.88	-56.66	-65.94
B2	-59.26		-60.05	-56.76	-66.70	-60.21	-64.59	-66.18	-56.76	-66.70
B3	-61.41	-59.30		-55.05	-64.57	-67.71	-65.89	-68.12	-55.05	-68.12
B4	-58.55	-59.00	-58.27		-66.07	-68.66	-66.80	-68.06	-58.27	-68.66
D1	-54.45	-62.05	-62.87	-60.51		-53.99	-54.03	-53.51	-53.51	-62.87
D2	-55.00	-61.72	-63.29	-60.70	-54.74		-54.30	-53.69	-53.69	-63.29
D3	-54.67	-62.14	-60.99	-59.06	-54.28	-53.78		-54.05	-53.78	-62.14
D4	-55.99	-64.50	-63.43	-61.18	-54.95	-53.47	-52.74		-52.74	-64.50
max	-54.45	-59.00	-58.27	-55.05	-54.28	-53.47	-52.74	-53.51	-52.74	
min	-61.41	-65.94	-63.43	-62.73	-66.70	-68.66	-66.80	-68.12		-68.66

	max	min	mean
coax-coax	-55.05	-65.94	-59.79
diff-diff	-52.74	-54.95	-53.96
coax-diff	-56.66	-68.66	-64.49
diff-coax	-54.45	-64.50	-60.16

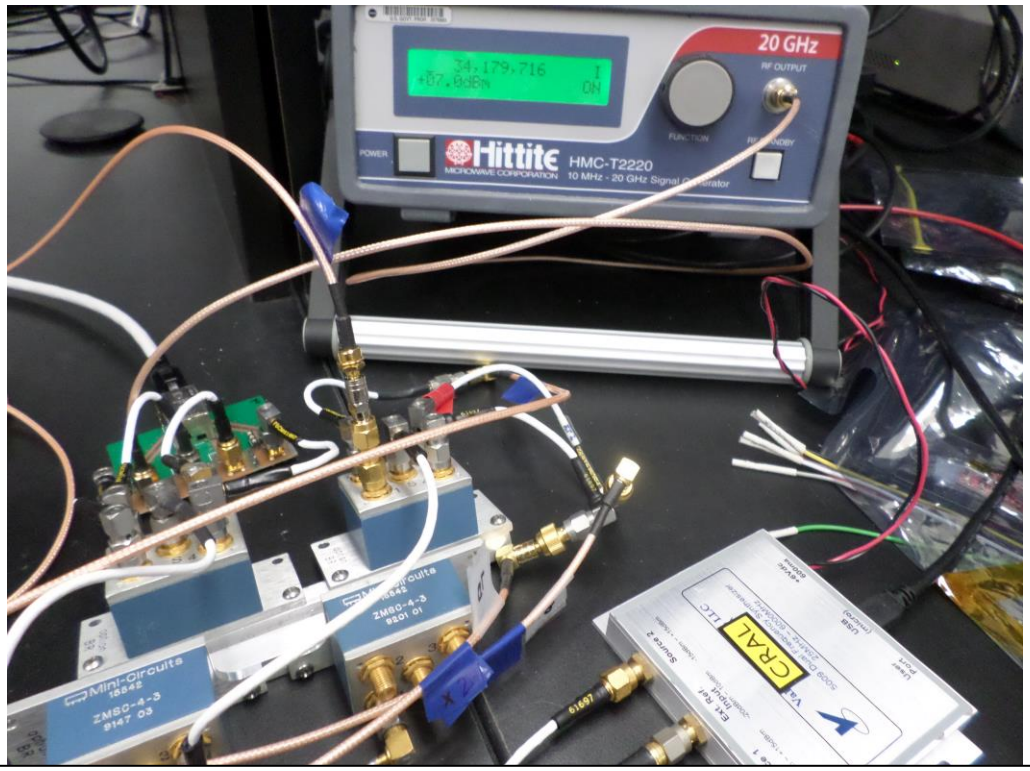

Figure 1: Photograph of part of the test setup. in the right foreground is the Valon 5009 synthesizer, and on the left is a set of four 1:4 power dividers (1 unused) for dividing the dither signal among 7 ADC inputs. Behind the power dividers is the SMA-to-ARJ45 breakout board.

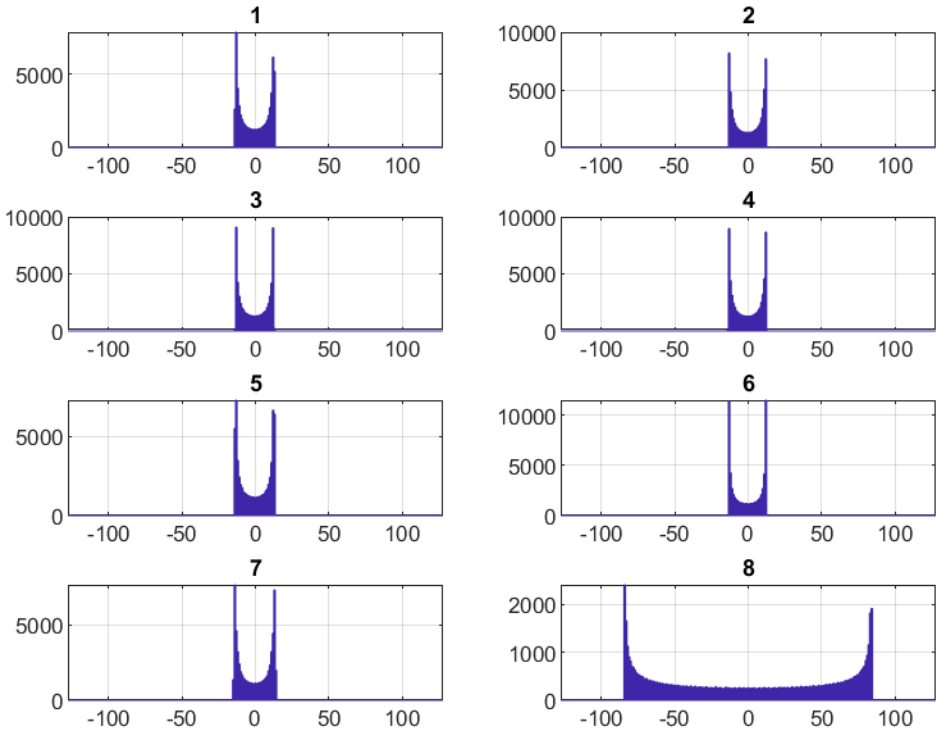

Figure 2: Typical set of histograms of the 65,536 samples from the 8 channels of two ADC devices. Channels 1-4 (B1-B4) are coax-connected and 5-8 (D1-D4) are differentially connected via ARJ45. In this case, the 34 MHz test signal was driving channel 8 at an amplitude of about 80 ADC counts, and the other channels were driven by the 97 MHz dither signal at an amplitude of about 8 counts.